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[ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS]

Abstract

Disclosed is an integrated circuit chip structure that has a chip level test access port (TAP) controller and a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have instruction register (IR) lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each, the chip level TAP includes a flexible length instruction register architecture adapted to accommodate the different length instruction registers of the embedded TAPs while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. Further, the invention includes selection logic adapted to actively connect only a single embedded TAP to the chip level TAP at a time.